國立中正大學 106 學年度碩士班招生考試試題

電磁晶片組

系所別：電機工程學系-計算機工程組

晶片系統組

光機電整合工程研究所

科目：電子學

第 2 節

1. (a) Use the Miller approximation to calculate the –3 dB frequency of the small-signal voltage gain of a differential stage as shown in Fig. P1, using these parameters: W = 100 μm, L_{drawn} = 2 μm, L_d = 0.2 μm, k' = 60 $\mu A/V^2$, R_S = 10 kΩ, R_L = 5 kΩ, I_1 = 1 mA, and f_T = 3 GHz (at I_D = 500 μA). Note that L_{drawn} is the channel length drawn in the layout, and L_d is the lateral diffusion length. (10%)

   (b) Calculate the non-dominant pole magnitude for the circuit in (a). (5%)

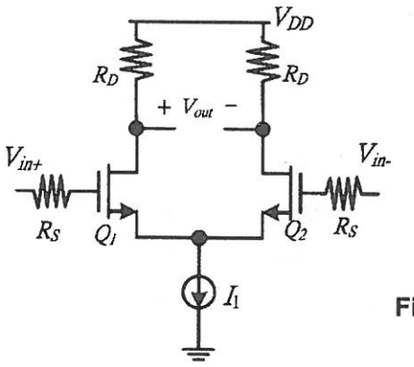

Fig. P1

2. Derive the output impedance R_{out} of the circuit shown in Fig. P2. Assume that all transistors have small-signal output resistance r_o and operate in saturation with transconductance g_m. (15%)

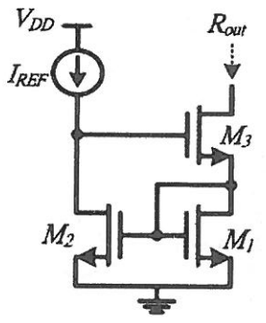

Fig. P2

3. The amplifier with feedback is shown in Fig. P3.
   (a) What is the feedback topology in this circuit?(3%)
   (b) Find the feedback factor. (4%)
   (c) Find the open-loop gain. (4%)
   (d) Find the closed-loop gain. (4%)
   (e) Find the closed-loop output impedance (5%)

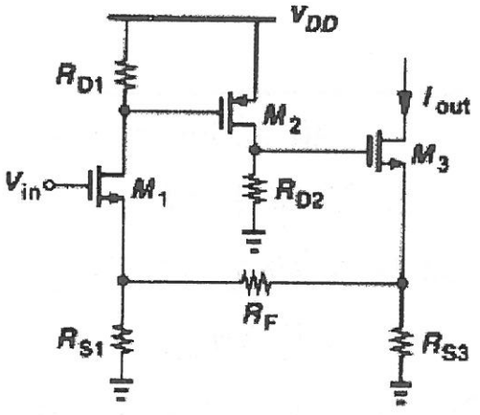

Fig. P3

4. In the circuits of Fig. P4(a) and Fig. P4(b), assume that the reverse saturation current is 5×10^{-16} A for each diode and the thermal voltage is 25 mV.

(a) In the circuit of Fig. P4(a), please calculate the current flowing through each diode. (5%)

(b) In the circuit of Fig. P4(b), please calculate the current flowing through the resistor. (8%)

(c) In the circuit of Fig. P4(c), please plot the input/output characteristic, assuming a 0.7-V constant-voltage drop model. (5%)

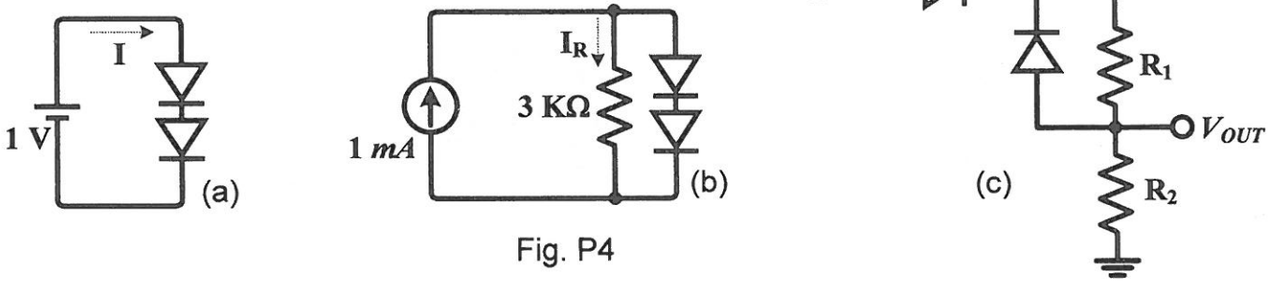

Fig. P4

5. The circuits in Fig. P5 is fabricated with the following process parameters: μ_nC_{ox} = 200 μA/V², μ_pC_{ox} = 100 μA/V², $V_{tn} = |V_{tp}|$ =0.4 V, and λ=0 V^{-1}.

(a) Please show that the drain current equals to $\mu_nC_{ox}\cdot\left(\frac{W}{L}\right)\cdot\left((V_{GS}-V_{tn})\cdot V_{DS}-\frac{1}{2}V_{DS}^2\right)$ for N-type MOSFET to operate in triode region. (5%)

(b) In the circuit shown in Fig. P5(a), compute W/L of Q_1 such that Q_1 can operate at the edge of saturation. Assume that the supply voltage V_{DD} is 1.8 V. (5%)

(c) To provide a voltage gain of 200 for the MOS cascode circuit of Fig. P5(b) with a bias current of 1 mA, please determine the transistor size of $(W/L)_{Q1}=(W/L)_{Q2}$. Assume that λ=0.1 V^{-1} in this case. (10%)

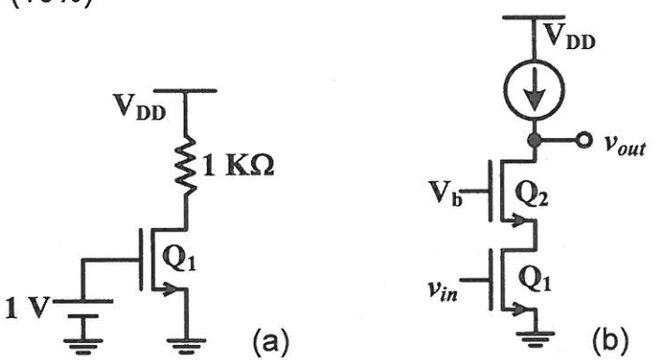

Fig. P5

6. (a) A CMOS logic gate is required to provide the function of $Y=\overline{(A+B)\cdot C+D\cdot(E\cdot F+G)}$, please sketch the schematic using MOS transistors. (4%)

(b) Please provide suitable transistor sizes for the circuit of (a) to have equal rise and fall times. Assume that $\mu_n=2\mu_p$. (4%)

(c) Please use a CMOS logic inverter to derive the dynamic power dissipation. Assume that the supply voltage, operating frequency, output load capacitance are V_{DD}, f, and C_L. (4%)