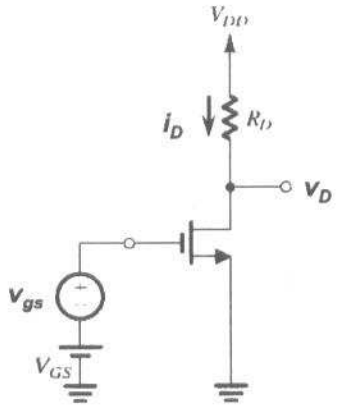
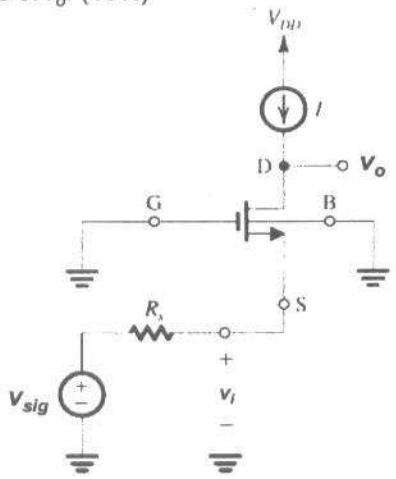
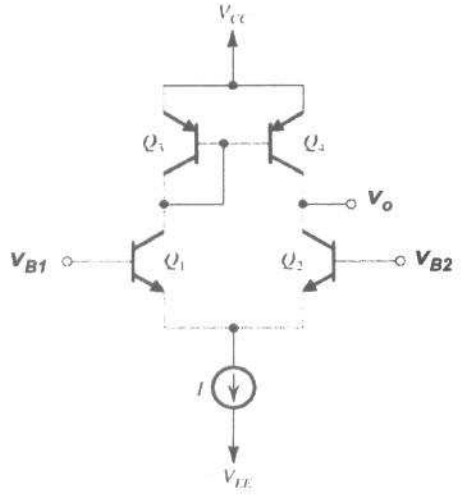
1. Consider the FET amplifier shown below, for which $V_t = 2$ V, $k_n'(W/L) = 1$ mA/V^2, $V_{GS} = 4$ V, $V_{DD} = 10$ V, and $R_D = 3.6$ kΩ. (17%)
   (a) Find the dc quantities I_D and V_D.
   (b) Calculate the value of g_m at the bias point.
   (c) Calculate the value of the voltage gain.
   (d) If the MOSFET has $\lambda = 0.01\text{V}^{-1}$, find r_o at the bias point and calculate the voltage gain.



2. A common-gate amplifier is specified to have $C_{gs} = 2$ pF, $C_{gd} = 0.1$ pF, $C_L = 2$ pF, $g_m = 5$ mA/V, $\chi = 0.2$, $R_S = 1$ kΩ, and $R_L = 20$ kΩ. Neglect the effects of r_o. (18%)
   (a) Find the low-frequency gain v_o / v_{sig}.
   (b) Find the frequencies of the poles f_{p1} and f_{p2}.
   (c) Estimate the 3-dB frequency f_H.

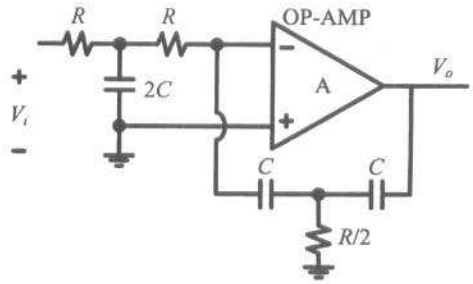


3. The differential amplifier shown below is operated with $I = 100$ μA, with devices for which $V_A = 160$ V, and $\beta = 100$. (20%)
   (a) Find the differential input resistance.
   (b) Find the differential output resistance.
   (c) Find the equivalent transconductance.
   (d) Find the open-circuit voltage gain.
   (e) What will the voltage gain be if the input resistance of the subsequent stage is 100 k Ω?



4. (6%)
(a) Please define the electron mobility.
(b) What is the difference between drift current and diffusion current?

5. Assume OP-AMP A in the circuit shown below is ideal. Find the transfer function V_o/V_i.(9%)



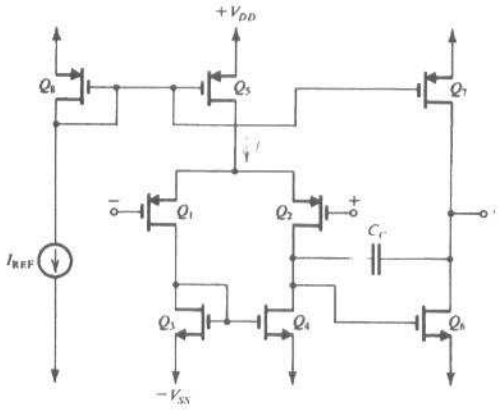
6. Consider the 6-bit charge-redistribution analog-to-digital converter with V_{REF} = 6 V. (10%)
(a) What is the voltage increment appearing on the top plate when S_5 is switched?
(b) What is the full-scale voltage of this converter?
(c) If the analog input V_A = 4.7 V, which switches will be connected to V_{REF} at the end of conversion?

7. A two-stage CMOS OP-AMP shown below is found to have a slew rate of 80 V/μs and a unity-gain bandwidth ft of 50 MHz. (10%)

(a) Estimate the value of the overdrive voltage at which the input-stage transistors are operating.

(b) If the first-stage bias current I = 120 μA, what value of miller compensation capacitor Cc must be used?

(c) For a process for which $\mu_p C_{ox}$ = 50 μA/V^2, what W/L ratio applies for Q_1 and Q_2?



8. (10%)

(a) Design and sketch the following Boolean function, using the CMOS logic gates.

$$Y = \overline{AB} + \overline{ACD}$$

(b) According to your design in (a), determine when will the worst propagation delay happen?

(c) Assume the channel length is 0.25 μm, and W/L ratios of the basic CMOS inverters are 1.5 and 5, for NMOS and PMOS respectively. Design the transistor W/L ratios for your logic circuits in (a) to make your circuits have equal propagation delay to basic CMOS inverters.