

1. (a) Plot the small-signal hybrid- $\pi$  model of the NMOS transistor. Label every component. (5%)  
 (b) Explain what causes channel-length modulation and how to lessen this non-ideal effect (5%)
2. Design a non-inverting amplifier, shown in Fig. P2, for the following specifications: closed-loop gain = 4, gain error = 1%, closed-loop bandwidth = 100MHz.  
 (a) Determine the required  $R_1$ ,  $R_2$ , and open-loop gain and bandwidth of the op amp. (8%)  
 (b) Explain what happens if op amp exhibits an offset of 20mV. (2%)

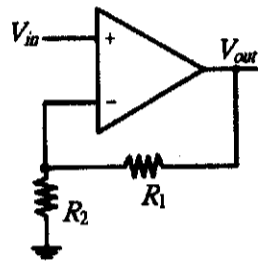


Fig. P2

3. Calculate the voltage gain of the circuit shown in Fig. P3.  $M_1$  is identical with  $M_2$ , and given  $V_{DD}=3V$ ,  $V_b=2V$ ,  $V_t=0.6V$ ,  $\mu_n C_{OX}(W/L)=240 \mu A/V^2$ ,  $I_1 = 3 \text{ mA}$ ,  $R_D = 0.5 \text{ k}\Omega$ , and  $\lambda = 0$ . (10%)

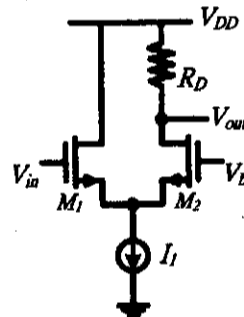


Fig. P3

4. A CMOS op amp, shown in Fig. P4, is found to have a slew rate of  $60 \text{ V}/\mu\text{s}$  and a unity-gain bandwidth  $f_t$  of 100 MHz.  
 (a) Estimate the value of the overdrive voltage of  $Q_1$  and  $Q_2$ . (5%)  
 (b) Given  $I_{D5} = 100 \mu\text{A}$ , calculate the value of  $C_C$ . (5%)  
 (c) A resistance  $R = 300\Omega$  is put in series with  $C_C$  to place the zero at infinite frequency. Calculate the required  $G_{m2}$ , which is the equivalent transconductance of the 2<sup>nd</sup> stage. (5%)  
 (d) What is the maximum allowed capacitance at  $v_o$  to have a  $75^\circ$  phase margin? (5%)

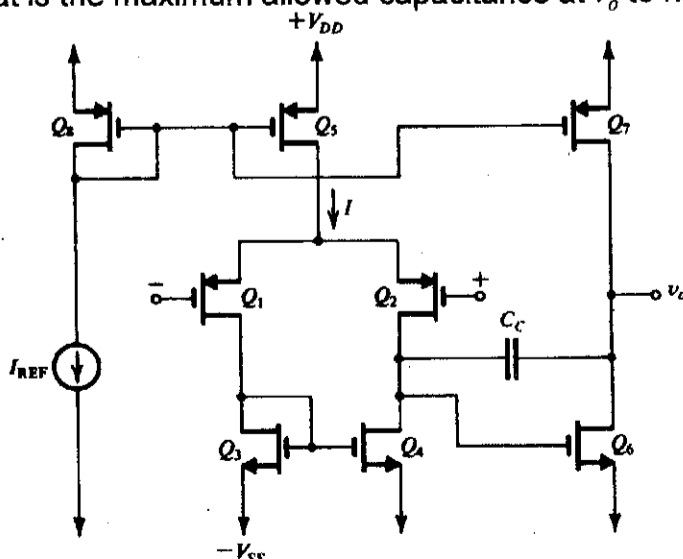
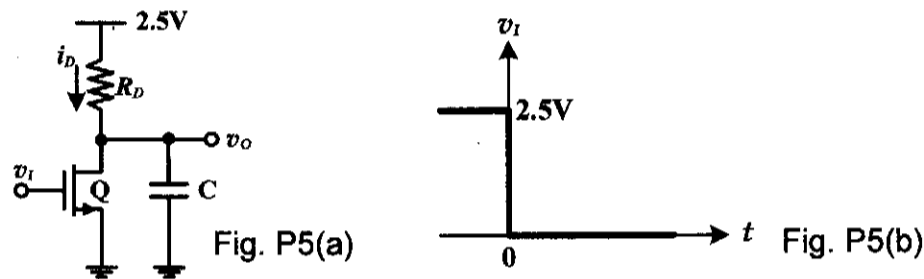


Fig. P4

5. Design of A Digital Logic Inverter (20%)

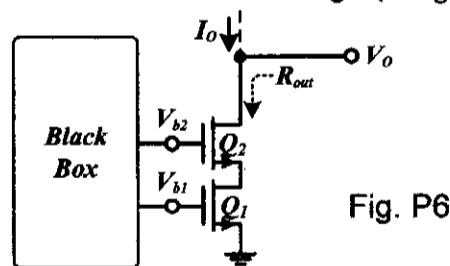
A digital logic inverter is shown in Fig. P5(a), and the transistor Q is fabricated with the following process parameters:  $C_{ox}\mu_n = 100 \mu A/V^2$ ,  $\lambda = 0$ , and  $V_{tn} = 0.5V$ .

- Please determine the W/L value of Q and resistance  $R_D$  to provide a 0.1V output low level ( $V_{OL}$ ) and a static current of  $100\mu A$ . (4%)
- As the circuit designated in (a), find the low-to-high propagation time ( $t_{PLH}$ ) if the load capacitance C in Fig. P5(a) is 100fF and  $v_i$  has a zero fall time as shown in Fig. P5(b). (4%)
- Please sketch the voltage transfer curve (VTC) of the circuit in Fig. P5(a) and use the VTC to explain the concept of noise margin. (4%)
- Use the known parameters to derive the expressions of the output high level ( $V_{OH}$ ), and the maximum value of input interpreted by the inverter as a logic 0 ( $V_{IL}$ ). (4%)
- How to improve the noise margin of the logic inverter shown in Fig. P5(a). (4%)



6. Assume that the circuit in Fig. P6 is designated to have a  $200k\Omega$  output resistance ( $R_{out}$ ) and a bias current of 0.5mA with the following process parameters:  $C_{ox}\mu_n = 100 \mu A/V^2$ ,  $\lambda = 0.1V^{-1}$ , and  $V_{tn} = 0.4V$ .

- If  $Q_1$  and  $Q_2$  are identical, find their W/L. (6%)
- Find the required value of  $V_{b1}$ . (5%)
- Complete a wide-swing current mirror circuit of Fig. P6 by exposing the possible circuitry in the Black Box and explain how the "wide-swing" is achieved. Note: wide-swing means that  $V_o$  is permitted to swing as low as two overdrive voltage ( $2V_{OV}$ ). (7%)



7. (a) Show the definition of slew rate (SR) of an operational amplifier. (5%)

- To produce a highest frequency of 1kHz and 10-V peak-to-peak sine wave at the output of an operational amplifier, what is the slew rate requirement of the operational amplifier? (7%)